Lab#9: Two Stage RC Coupled Transistor Amplifier

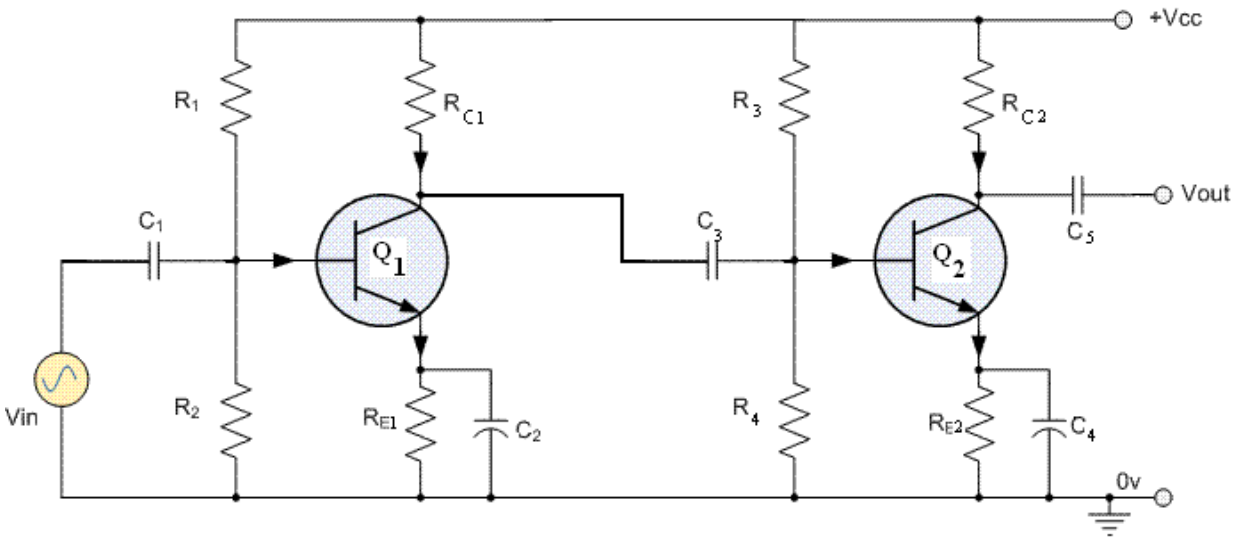
Objectives:

1. To design a two stage RC coupled common emitter transistor (NPN) amplifier circuit and to study its frequency response curve.

Overview:

A single stage of amplification is often not enough for a particular application. The overall gain can be increased by using more than one stage, so when two amplifiers are connected in such a way that the output signal of the first serves as the input signal to the second, the amplifiers are said to be connected in *cascade.* The most common arrangement is the common-emitter configuration.

Resistance-capacitance (RC) coupling is most widely used to connect the output of first stage to the input (base) of the second stage and so on. It is the most popular type of coupling because it is cheap and provides a constant amplification over a wide range of frequencies. These R-C coupled amplifier circuits are commonly used as voltage amplifiers in the audio systems.



The circuit diagram above shows the 2-stages of an R-C coupled amplifier in CE configuration using NPN transistors. Capacitors C_1 and C_3 couple the input signal to transistors Q_1 and Q_2, respectively. C_5 is used for coupling the signal from Q_2 to its load. R_1, R_2, R_{E1} and R_3, R_4, R_{E2} are used for biasing and stabilization of stage 1 and 2 of the amplifier. C_2 and C_4 provide low reactance paths to the signal through the emitter.

Overall gain:

The total gain of a 2-stage amplifier is equal to the product of individual gain of each stage. (You may refer to the handout for single stage amplifier to calculate individual gain of the stages.) Once the second stage is added, its input impedance acts as an

additional load on the first stage thereby reducing the gain as compared to its no load gain. Thus the overall gain characteristics is affected due to this loading effect.
The loading of the second stage i.e. input impedance of second stage, $\mathbf{Z_{i2} = R_3 \parallel R_4 \parallel \beta r_{e2}}$

Thus loaded gain of the first stage, $A_{V1} = -\dfrac{R_{C1} \parallel Z_{i2}}{r_{e1}}$

and the unloaded gain of second stage, $A_{V2} = -\dfrac{R_{C2}}{r_{e2}}$

In the circuit diagram provided below, the emitter resistor is split into two in order to reduce the gain to avoid distortion. So the expression for gain each stage is modified as

$$A_{V1} = -\frac{R_{C1} \parallel Z_{i2}}{(R_{E1} + r_{e1})}$$

$$A_{V2} = -\frac{R_{C2}}{R_{E2} + r_{e2}}$$

The overall gain of the 2 stage amplifier is $A_V = A_{V1} \times A_{V2}$.

Frequency Response Curve

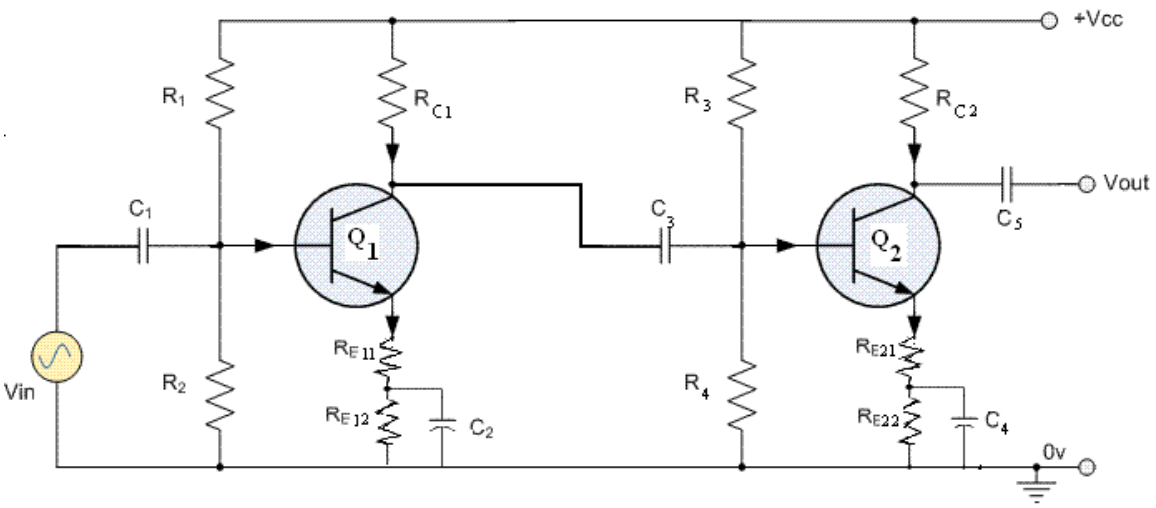
The performance of an amplifier is characterized by its frequency response curve that shows voltage gain (often expressed in dB units) plotted versus frequency. The frequency response begins with the lower frequency region designated between 0 Hz and lower cutoff frequency. At lower cutoff frequency, f_L , the gain is equal to 0.707 A_{mid}. A_{mid} is a constant mid-band gain obtained from the mid-band frequency region. The third, the upper frequency region covers frequency between upper cutoff frequency and above. Similarly, at upper cutoff frequency, f_H, the gain is equal to 0.707 A_{mid}. Beyond the upper cutoff frequency, the gain decreases as the frequency increases and dies off eventually. (More details are given in the hand out for single stage amplifier.)

Design: The design details are already given in the single stage amplifier hand out.

Components/ Equipments:

1. Transistor: CL100 (or equivalent general purpose npn, 2 nos)
2. Resistors: R_1, R_3= 26 (27) KΩ, R_2, R_4= 5 (4.7+0.22) KΩ, $R_{C\,1}$, R_{C2}= 4 (3.9) KΩ, R_{E1}, R_{E2}= 1kΩ (R_{E11}, R_{E21}=470 Ω; R_{E12}, R_{E22}=560 Ω) (2 nos. of each resistance value)
3. Capacitors: C_1= C_3= C_5= 1 μF (3 nos.), C_2= C_4= 100μF (2 nos.)
4. Power Supply (V_{CC} = 12V)
5. Oscilloscope
6. Function Generator (~ 100-200 mV pp, sinusoidal for input signal)
7. Breadboard
8. Connecting wires

Circuit Diagram:



Procedure:

1. Measure and record all the values of resistance and capacitance and β of the transistor using a multimeter. Configure the circuit as per the diagram. Make a provision so that the two stages can either be separated or connected as and when required.
2. Apply supply voltage to the circuit. Measure and record all the dc parameters of each individual stage separately as listed in Table 1 in absence of the ac signal.
3. Next, set the function generator at **20kHz by putting the frequency knob in 20KHz range and adjusting the variable knob.** Also, set the "Attenuation" button at 40dB. Connect the output to the oscilloscope and adjust the "Amplitude" knob till you get a sinusoidal input signal, Vi ≈ 100-200 mV peak-to-peak value. DO NOT CHANGE THIS SETTING THROUGHOUT THE EXPERIMENT.
4. To fill up first row of Table 2 the two stages should be separated. Now apply the input signal to the circuit at the first stage keeping the connection to oscilloscope intact. Feed the output of the first stage to the other channel of oscilloscope. Take care to make all the ground pins common. Measure the output and calculate unloaded gain of stage 1.
5. Similarly by applying input at the second stage measure the output and calculate the unloaded gain of second stage.
6. For the second row of Table 2, connect the two stages. Apply the input signal at the first stage Measure the output of first stage and calculate its loaded gain.
7. Now, with the input signal at the first stage, measure the output at the second stage and calculate the total gain of the two stage amplifier and complete Table-2.
8. To study the frequency response of the two stage amplifier, vary the input signal frequency in the range 20 Hz – 2 MHz, keeping the input signal amplitude always constant. Observe measure and record the output voltage, V_o at the second stage. (You may have to measure V_i and take the ratio V_o/V_i each time in case input fluctuation is too large to hold constant.) Calculate voltage gain for each frequency.

9. Plot the frequency response curve, i.e. voltage gain in dB versus frequency on a semi-log graph-sheet.
10. Estimate the mid-frequency gain and also the lower and higher cut off frequencies and hence the bandwidth.

Observations:

$\beta 1$ = _____ , $\beta 2$ = _____

Stage 1: R_1= ____, R_2= ____, R_C= ____, R_E= ____+___; C_1= ___, C_2= ___, C_E= ___
Stage 2: R_1= ____, R_2= ____, R_C= ____, R_E= ____+___; C_1= ___, C_2= ___, C_E= ___

Table 1: D.C. analysis of the circuit

V_{CC} = 12V

Parameter	Stage 1 (Q1)		Stage 2 (Q2)	
	Computed value	Observed value	Computed value	Observed value
V_B (V)				
V_E (V)				
$I_C \approx I_E$ (mA)				
V_{CE} (V)				
r_e(Ω)				
Q-point				

Table 2: Mid frequency voltage Gain ($f \approx$ 20 kHz)

Vi = _____

Parameter	Stage 1 (Q1)		Stage 2 (Q2)	
	Computed	Measured	Computed	Measured
Unloaded Voltage Gain (V_o/ V_i)				
Loaded Voltage Gain				

Total mid frequency gain = Loaded Voltage Gain (Q1) × Unloaded Voltage Gain (Q2)

Total gain (computed) = _____

Total gain (measured) = _____

Table 3: Frequency Response

$V_i(pp)$ = _____

Sl. No.	Frequency, f (kHz)	$V_0(pp)$ (Volt)	Gain,$A_V = \frac{V_o(pp)}{V_i(pp)}$	Gain (dB)
1				
2				
..				
..				

Calculations: Stage 1: Z_{i1} = _____, Z_{o1} = _____

Stage 2: Z_{i2} = _____, Z_{o2} = _____

Graphs: Plot the frequency response curve and determine the cut-off frequencies, bandwidth and mid-band gain.

Discussions:

Precautions:

1. Vary the input signal frequency slowly.
2. Connect electrolytic capacitors carefully.

Reference: Electronic devices and circuit theory, Robert L. Boylestad & Louis Nashelsky (10^{th} Edition)